SYSC3601
Microprocessor Systems

Unit 2a:
The Intel x86 Protected Mode

Topics/Reading

1. Protected Mode (Ch 2.3)

Protected Mode

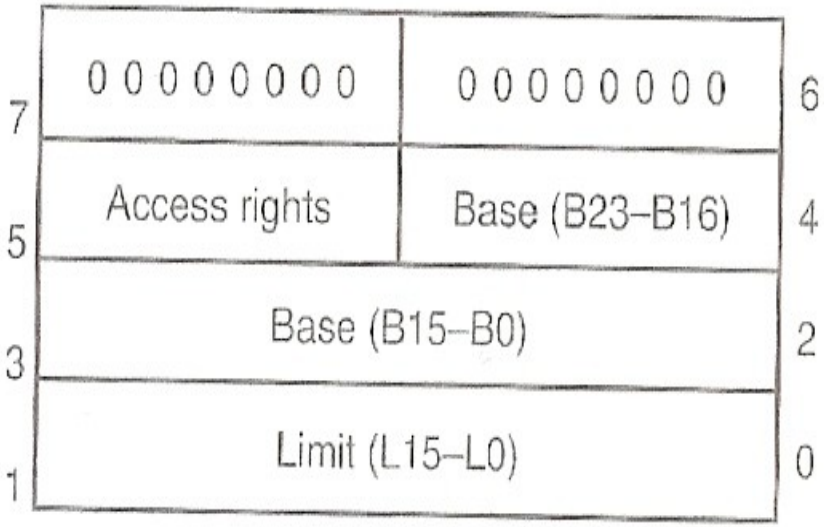
- The Windows operating system domain.
- 4G of memory with 2G for the system and 2 G for the application
- Protected mode still uses segment and offset addresses, but the offset address is 32-bits
- Protection is provided by restricting access through priority levels and access rights

Descriptors Describe Memory

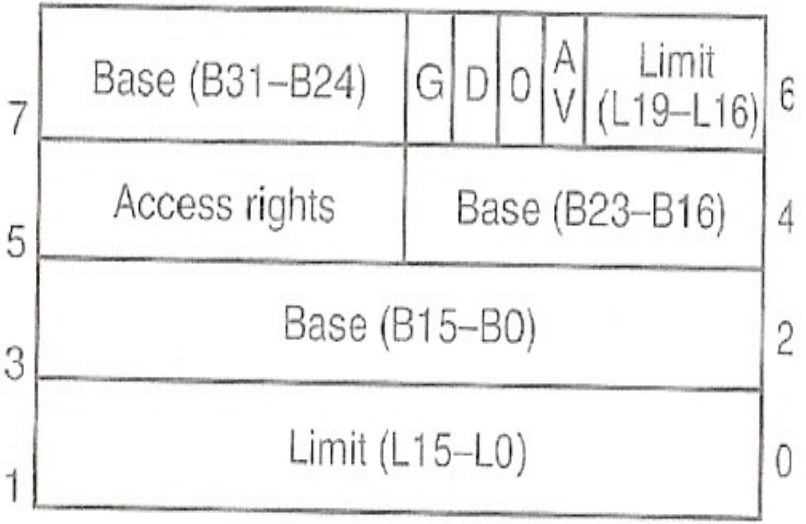
- A descriptor is selected by the number placed in the segment register.
- The descriptor describes the base address (starting address) and limit (offset to the ending address) of a segment.
- The descriptor also defines the privilege level and access rights to a memory segment.

Descriptor Table Entry Format

80286 descriptor



80386 through Pentium 4 descriptor



Descriptor Table Entry Format

- The base address is a 32-bit address (Pentium class) that addresses the start of a memory segment.
- The limit is a 20-bit number added to the base address to address the last address of a segment.
- The limit has a modifier bit called Granularity (G) that select a multiplier of 4K for the limit (4K is 12-bits)

  (20-bits +12-bits is 32-bits)

Descriptor Table Entry Example

- base = 23000000H and a limit of 012FFH

  G = 0 (limit = 000012FFH)

  Segment start = 23000000H

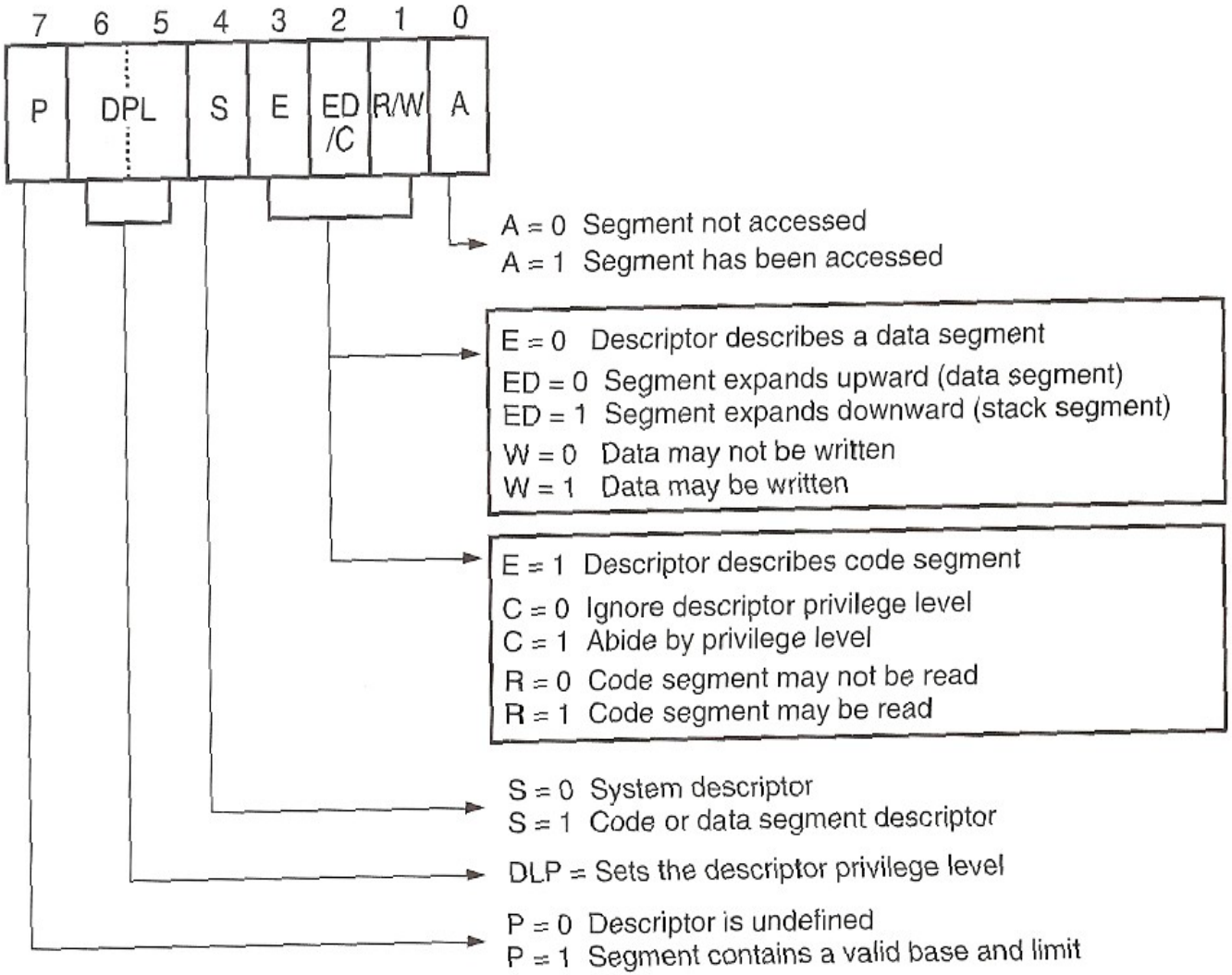
  Segment end = 230012FFH

  G = 1 (limit = 012FFFFFH)

  Segment start = 23000000H

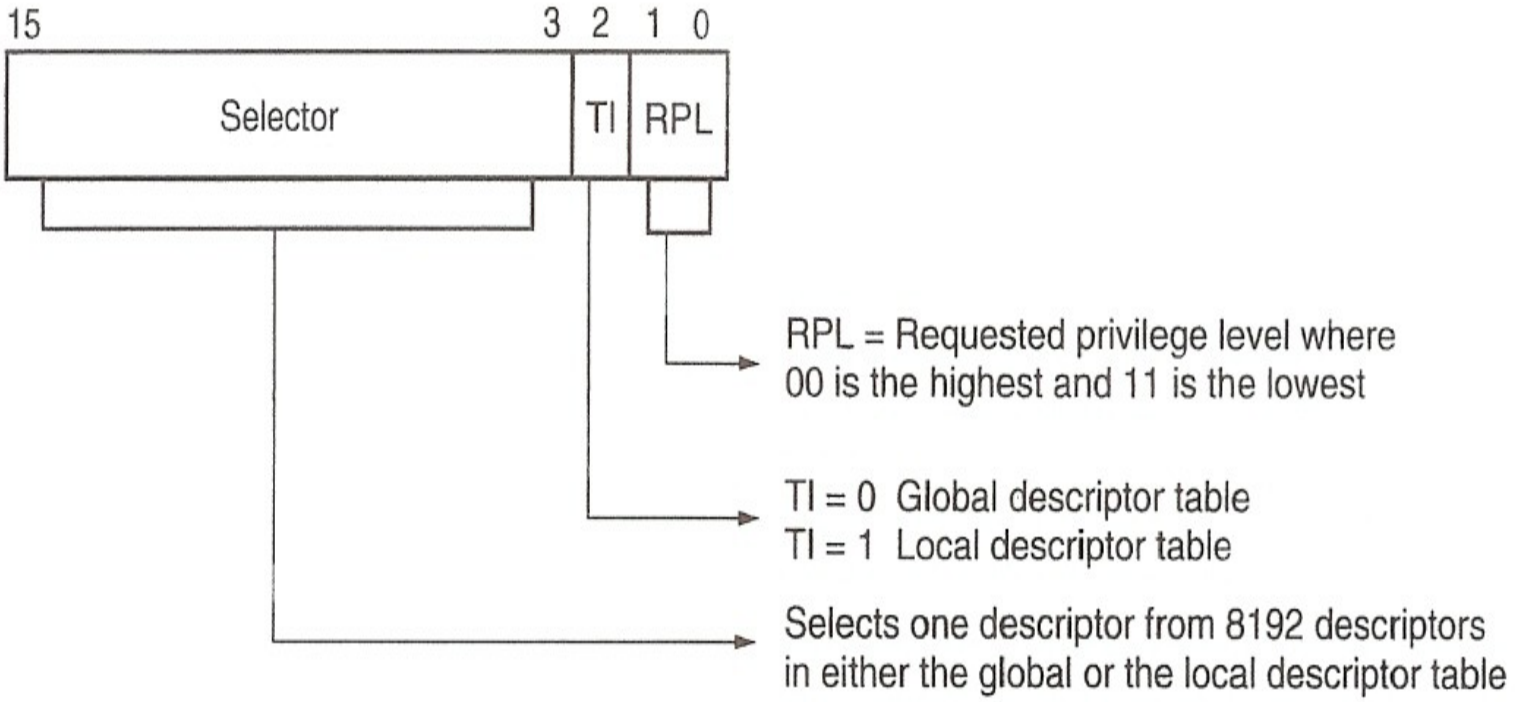
  Segment end = 242FFFFFH

Access Rights

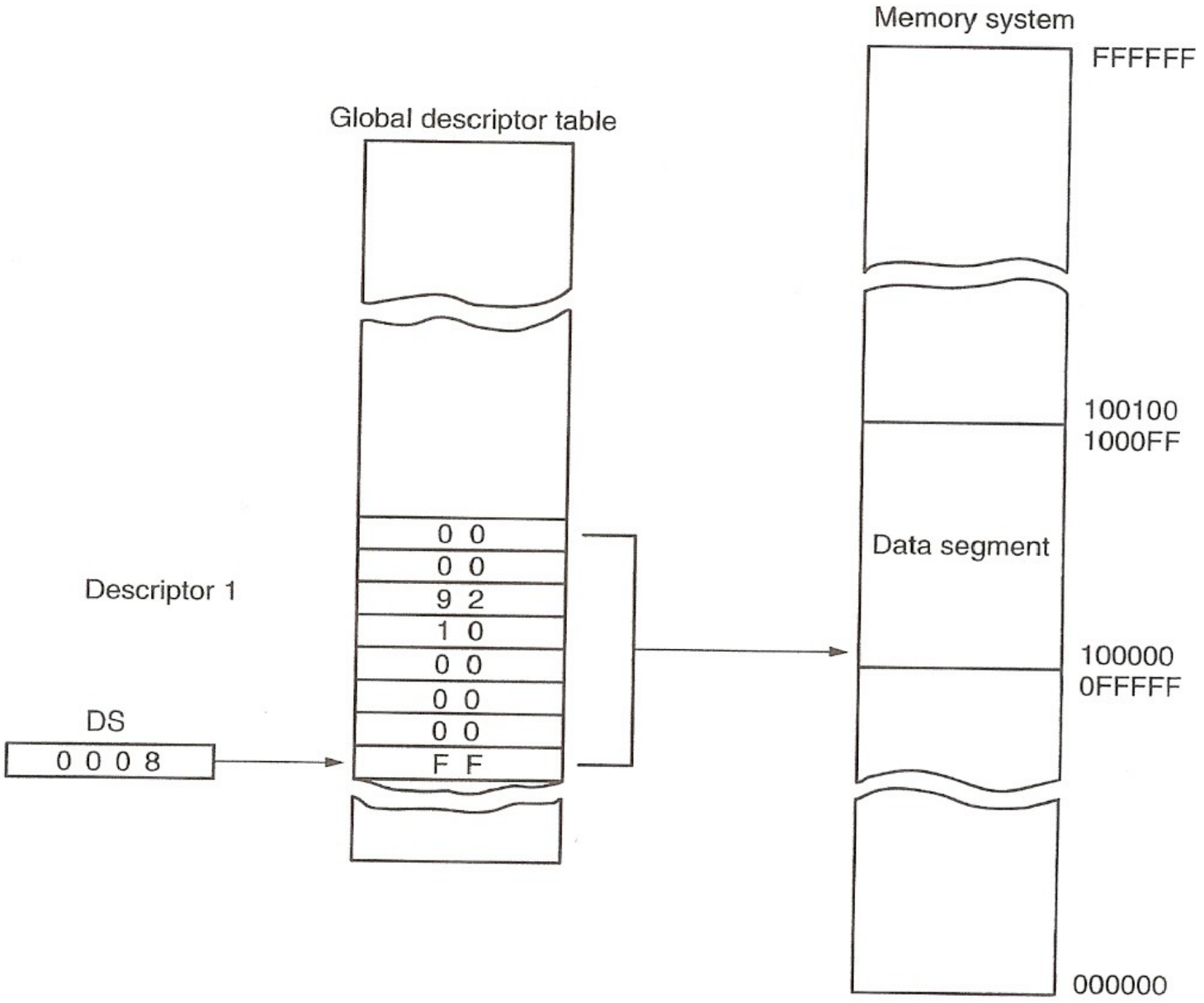


Note: Some of the letters used to describe the bits in the access rights bytes vary in Intel documentation.

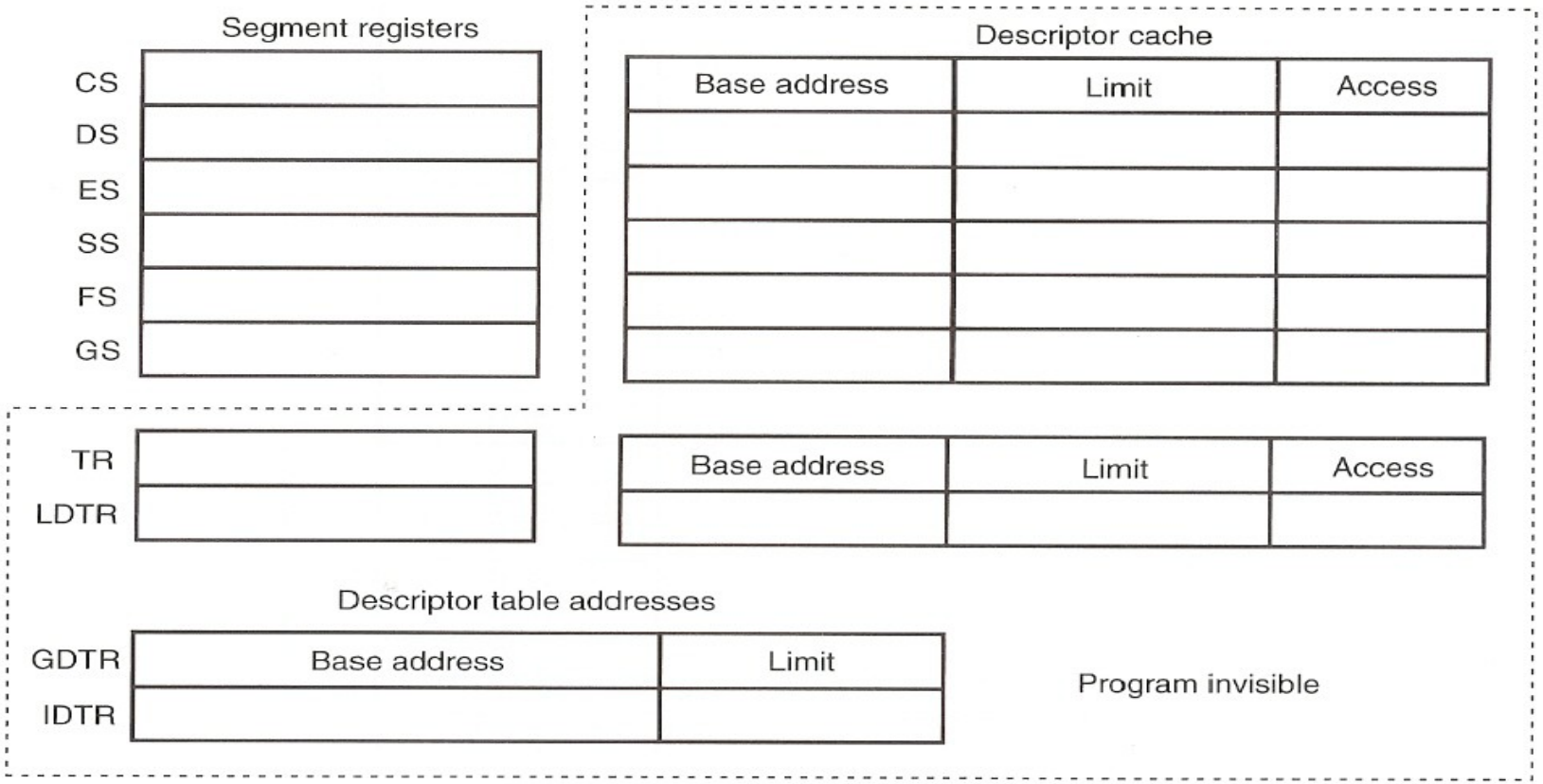
Segment Register



Segment Register Example



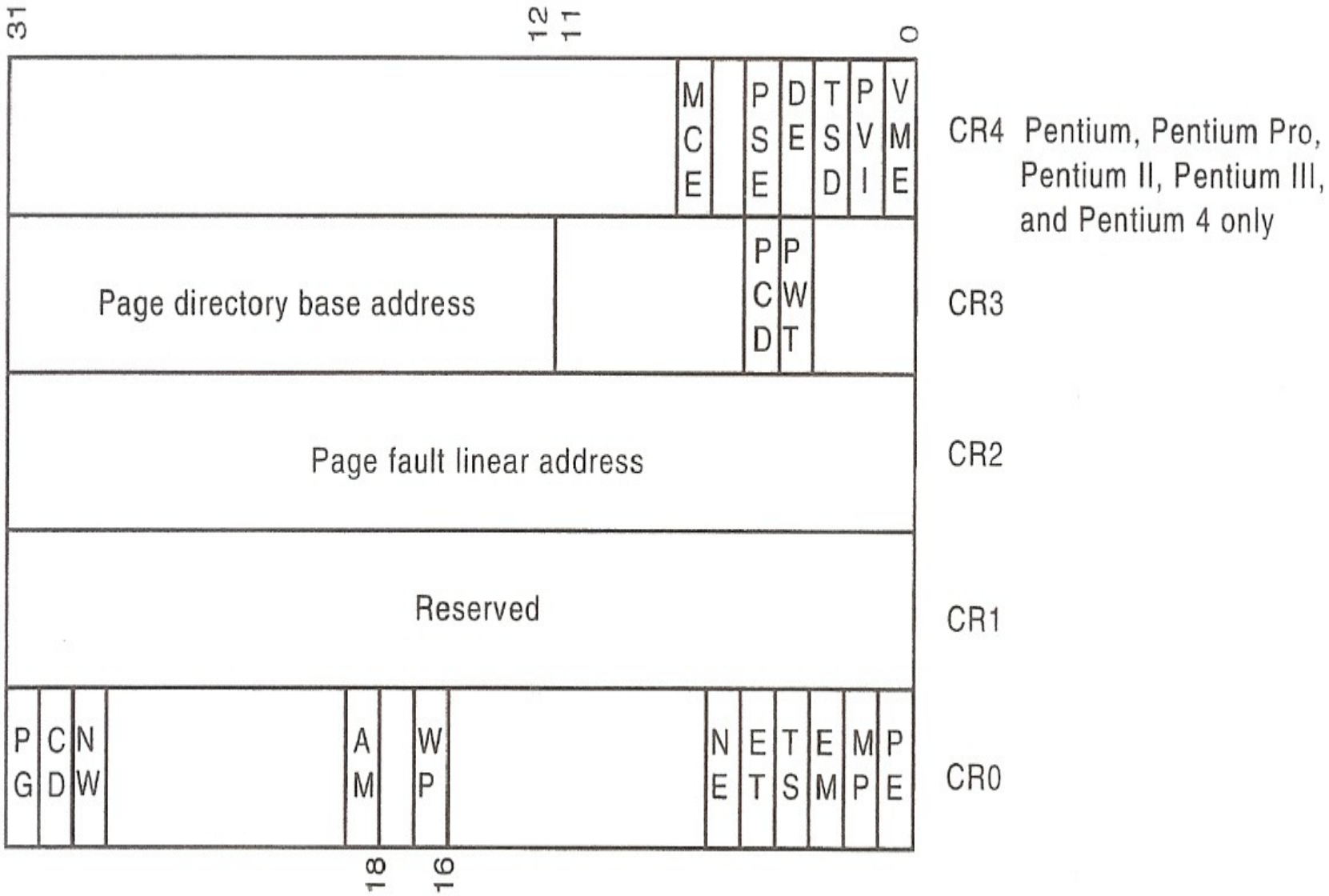
Program Invisible Registers



Notes:

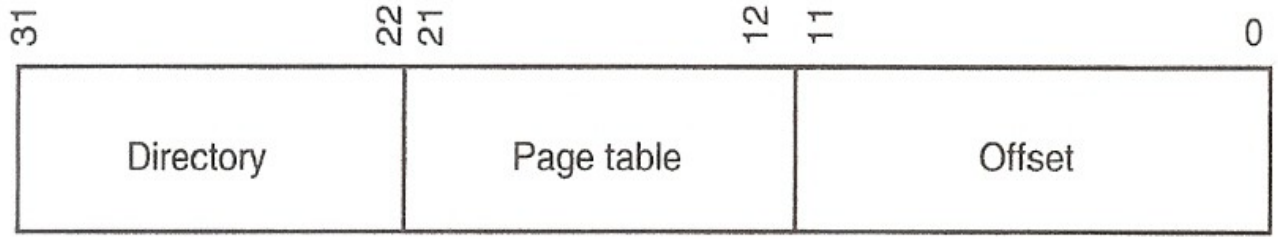
1. The 80286 does not contain FS and GS nor the program-invisible portions of these registers.
2. The 80286 contains a base address that is 24-bits and a limit that is 16-bits.
3. The 80386/80486/Pentium/Pentium Pro contain a base address that is 32-bits and a limit that is 20-bits.
4. The access rights are 8-bits in the 80286 and 12-bits in the 80386/80486/Pentium.

Control Registers

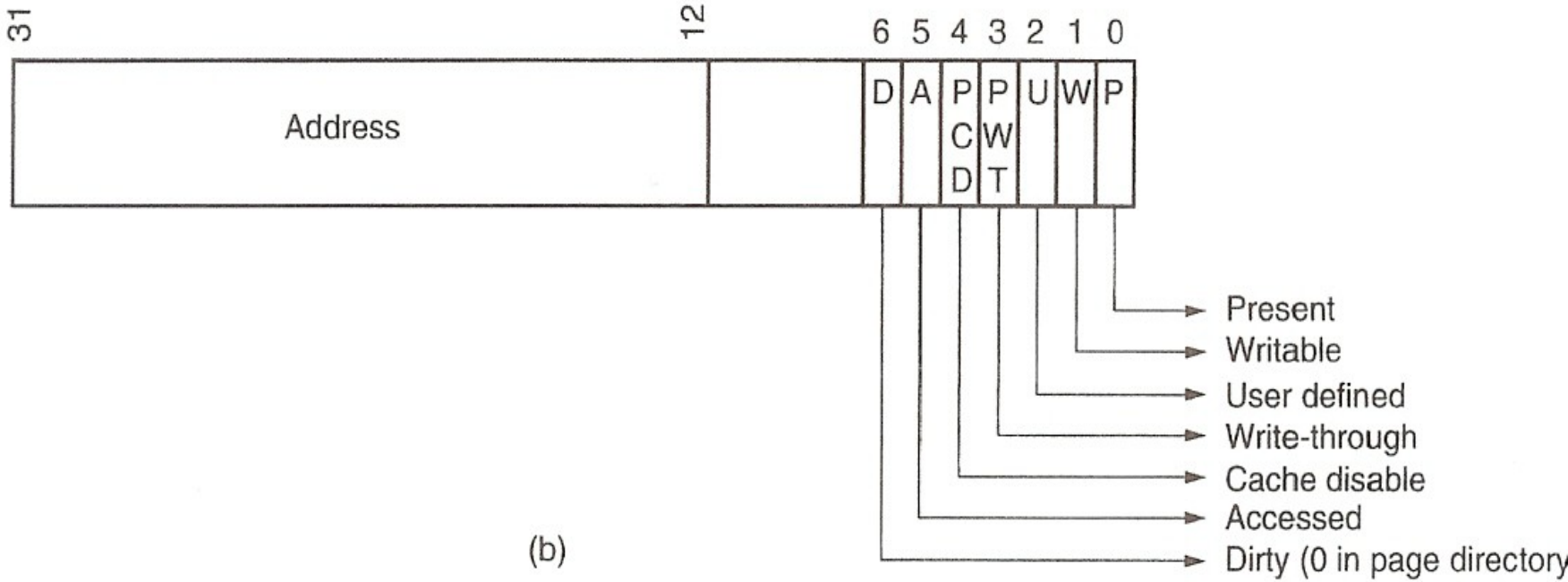


Paging

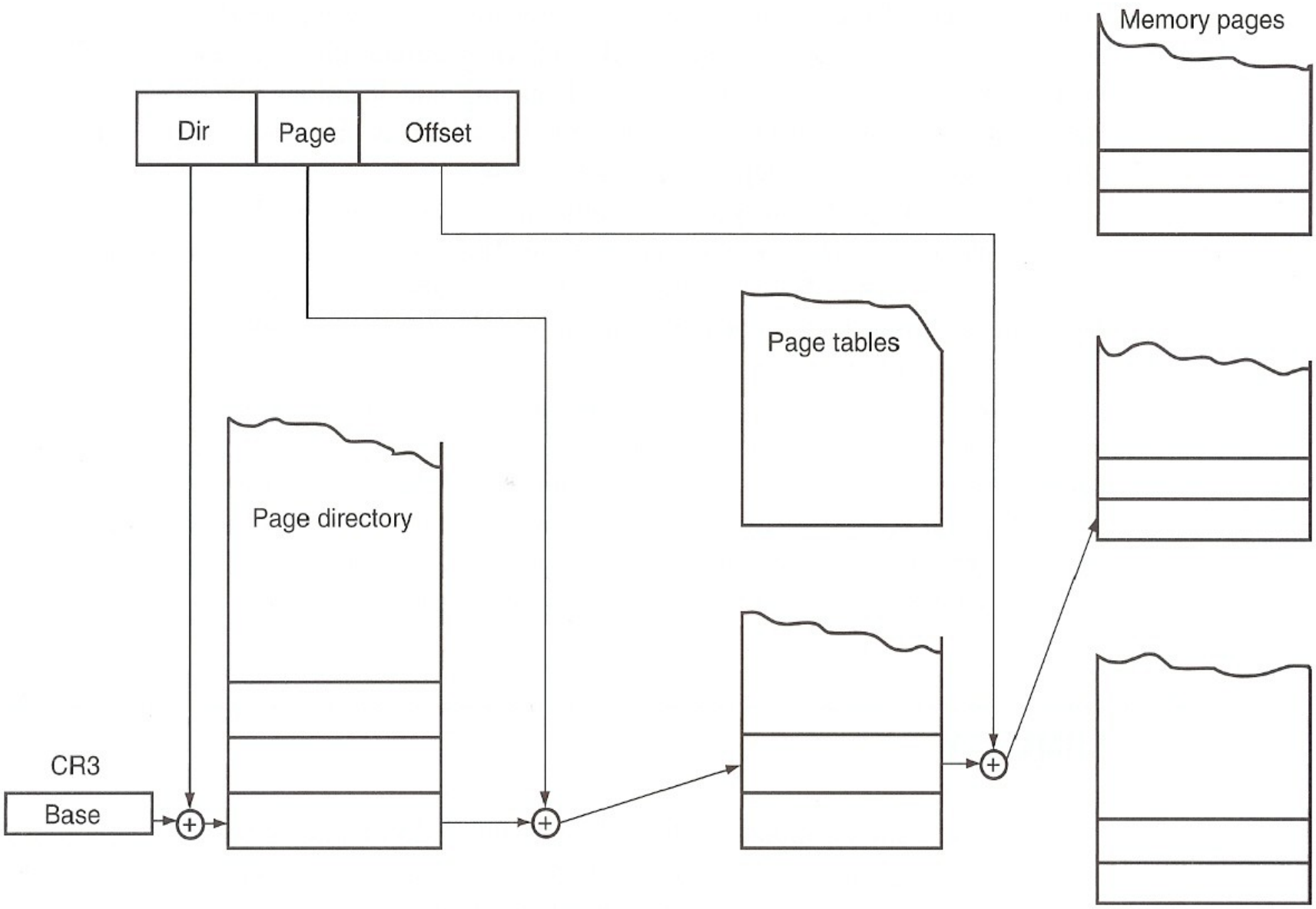
- The paging mechanism translates a logic address (address generated by the program) into a physical address (address that accesses a memory location).
- It does this by sectioning the address into three parts: (1) directory, (2) page table, and (3) memory offset.
- The directory and page table fields are each 10-bits wide and the memory offset is 12-bits.


31
22
21
12
11
0
Directory
Page table
Offset

(a)


31
12
6 5 4 3 2 1 0
Address
D
A
PCD
PWT
U
W
P
Present
Writable
User defined
Write-through
Cache disable
Accessed
Dirty (0 in page directory

(b)


Memory pages
Dir
Page
Offset
Page tables
Page directory
CR3
Base